



Data Sheet

VT1632A DVI Transmitter Flat Panel Display Interface

(Released under Creative Commons License)
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VIA TECHNOLOGIES, INC.

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VT1632A

DVI Transmitter

Flat Panel Display Interface

PRODUCT FEATURES

- **Standard Compliant with DVI 1.0**
- **25 to 165 MHz Input Clock Support**
- **Supports Panel Resolution from VGA through UXGA (1600 x 1200)**
- **Supports both 12-bit and 24-bit Input Modes**
- **Low Voltage Digital Interface**
- **De-Skewing Option for Varying the Input Clock-To-Data Timing**
- **I²C Slave Programming Interface**
- **Up to 5m Twisted Pair and Fiber Optical Ready**
- **Hot Plug Detection Input**
- **Low Power 3.3V Operation and Power Down Mode**
- **64-Pin TQFP Package**

OVERVIEW

The VT1632A DVI transmitter is designed to be compliant with DVI 1.0 (DVI is backwards compliant with VESA P&D and DFP) and supports flat panel displays ranging from VGA to UXGA resolutions (25 to 165Mpps) in a single link interface. Three DVI data channels send data at up to 1.65Gbps per channel.

Besides being able to be programmed through an I²C interface, the VT1632A is featured with Receiver and Hot Plug Detection. It also contains a highly flexible interface with either a 12-bit mode (1/2 pixel per clock edge) or a 24-bit mode 1 pixel per clock input for true color (16.7Million) support. In the 24-bit mode, the VT1632A supports single or dual edge clocking; in the 12-bit mode, it supports dual edge single clocking or single edge dual clocking.

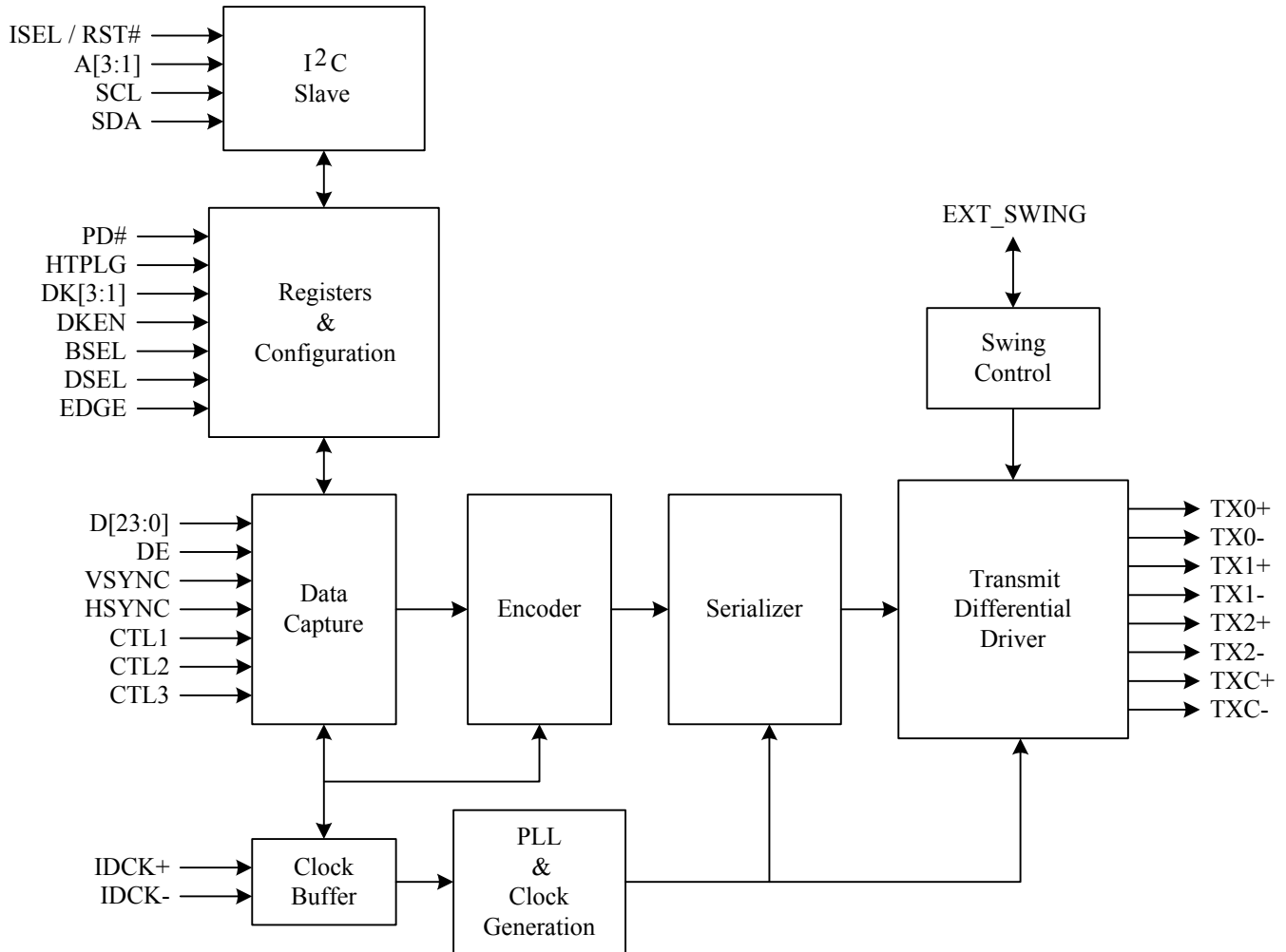


Figure 1. Functional Block Diagram

PINOUPS

Pin Diagram

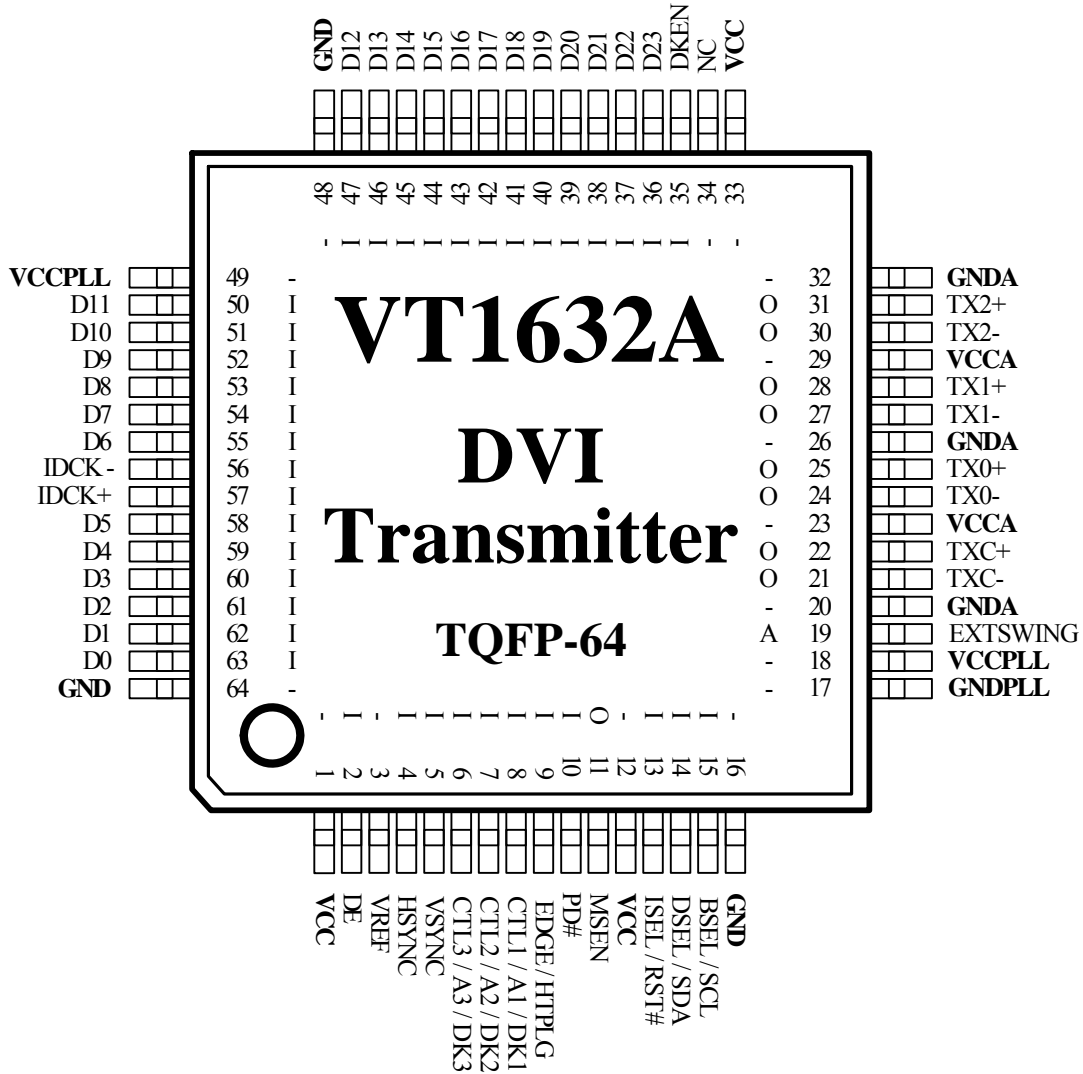


Figure 2. Pin Diagram (Top View)

Pin List
Table 1. Pin List (Alphabetical Order)

Pin	I/O	Pin Name	Pin	I/O	Pin Name
15	I	BSEL / SCLK	19	AI	EXTSWING
8	I	CTL1 / A1 / DK1	16	P	GND
7	I	CTL2 / A2 / DK2	48	P	GND
6	I	CTL3 / A3 / DK3	64	P	GND
63	I	D00	20	P	GND _A
62	I	D01	26	P	GND _A
61	I	D02	32	P	GND _A
60	I	D03	17	P	GNDPLL
59	I	D04	4	I	HSYNC
58	I	D05	56	I	IDCK-
55	I	D06	57	I	IDCK+
54	I	D07	13	I	ISEL / RST#
53	I	D08	11	O	MSEN
52	I	D09	34	-	NC
51	I	D10	10	I	PD#
50	I	D11	24	AO	TX0-
47	I	D12	25	AO	TX0+
46	I	D13	27	AO	TX1-
45	I	D14	28	AO	TX1+
44	I	D15	30	AO	TX2-
43	I	D16	31	AO	TX2+
42	I	D17	21	AO	TXC-
41	I	D18	22	AO	TXC+
40	I	D19	1	P	VCC
39	I	D20	12	P	VCC
38	I	D21	33	P	VCC
37	I	D22	23	P	VCCA
36	I	D23	29	P	VCCA
2	I	DE	18	P	VCCPLL
35	I	DKEN	49	P	VCCPLL
14	I	DSEL / SDA	3	AI	VREF
9	I	EDGE / HTPLG	5	I	VSYNC

Pin Descriptions
Table 2. Pin Descriptions

Input Pins			
Signal Name	Pin #	Type	Description
D[23:12]	36-47	I	Pixel Bus Upper. If BSEL = High, these 12 bits are used for pixel data input as the upper half of the 24-bit pixel bus. If BSEL = Low, these bits are not used for pixel data input. In the 12-bit mode, the state of D[23:16] is input to the I ² C register, CFG. Thus, the graphics controller can read 8 bits of user configuration data through the I ² C interface (see the I ² C register table in page 11 for more information). In the 12-bit mode, D[15:12] are reserved for VIA use only and should be tied to GND when not in use.
D[11:0]	50-55, 58-63	I	Pixel Bus Lower. If BSEL = High, these 12 bits are used for pixel data input as the lower half of the 24-bit pixel bus. When BSEL = Low, this bus inputs ½ a pixel (12 bits) at every latch edge (both falling and/or rising) of the clock.
IDCK+ IDCK-	57 56	I I	Input Data Clock. The minus clock input, IDCK-, is used only in 12-bit mode when dual edge clocking is turned off (DSEL = Low). The minus clock input provides the odd latching edges for dual clock single edge. If (BSEL = High) or (DSEL = High), the IDCK- pin is unused and should be tied to GND.
DE	2	I	Data Enable. When input pixel data is valid to the transmitter, DE = High; otherwise, DE = Low. It is important that this signal should have the same setup / hold timing as the data bus.
HSYNC	4	I	Horizontal Sync.
VSYNC	5	I	Vertical Sync.
CTL1 / A1 / DK1 CTL2 / A2 / DK2 CTL3 / A3 / DK3	8 7 6	I	MultiFunction Pins. The use of these multi-function input pins are dependent on the settings of ISEL and DKEN. These pins are regular high-swing 3.3V CMOS level inputs. These pins contain weak pull-down resistors so that if left unconnected, they will be Low. <u>ISEL=Low, DKEN=Low:</u> General Purpose Input CTL[3:1] are active. These pins are used for backward compatibility. These pins must be used to send DC signals only during the blanking time. <u>ISEL=Low, DKEN=High:</u> DK[3:1] are active. These pins are used to select the de-skew setting for the input bus. <u>ISEL=High, DKEN=Do not Care:</u> A[3:1] are active. These pins are used to set the lower 3 bits of the I ² C device address.

Status Pin			
Signal Name	Pin #	Type	Description
MSEN	11	O	Monitor Sense. The behavior of this open collector output pin is dependent on whether the status of the I ² C interface is enabled or disabled: <u>I²C bus disabled (ISEL = Low):</u> A High level indicates a powered on receiver being detected at the differential outputs. A Low level indicates a powered on receiver not being detected. This function can only be used in DC-coupling systems. <u>I²C bus is enabled (ISEL = High):</u> The output is programmable through the I ² C interface (see I ² C register definitions). An external 5K pull-up resistor is required on this pin for systems without an internal pull-up resistor.

Configuration / Programming Pins			
Signal Name	Pin #	Type	Description
ISEL / RST#	13	I	I²C Interface Select / I²C Reset. If this input is high, then the I ² C interface is active. If this input is low, the I ² C interface is inactive and the chip configuration is read from the configuration strapping pins. This pin also serves as an asynchronous reset to the I ² C interface controller. Reset is active when this input is held Low. Note: When the I ² C interface is active, DKEN must be set High.
BSEL / SCL	15	I	Input Bus Select / I²C Clock. When the I ² C bus is enabled (ISEL = High), this pin is the I ² C clock input. When the I ² C is disabled (ISEL = Low), this pin is used to select the input bus width. <u>Input Bus Select:</u> Set High to select 24-bit input mode Set Low to select 12-bit input mode
DSEL / SDA	14	I	Dual Edge Clock Select / I²C Data. When the I ² C bus is enabled (ISEL = High), this pin serves as the I ² C data input. When the I ² C bus is disabled (ISEL = Low), this pin selects whether single clock dual edge is used. <u>Dual Edge Clock Select:</u> When set High, IDCK+ latches input data on both falling and rising clock edges. When set Low, IDCK+/IDCK- latches input data on only falling or rising clock edges. <u>12/24-bit Mode:</u> If set High (dual edge), IDCK+ is used to latch data on both falling and rising edges. If set Low (single edge), IDCK+ latches 1 st half data and IDCK- latches 2 nd half data.
EDGE / HTPLG	9	I	Edge Select / Hot Plug. When the I ² C bus is enabled (ISEL = High), this pin is used to monitor the “Hot Plug” detect signal (refer to the DVI TM or VESA [®] P&D TM and DFP standards). NOTE: This is a 3.3V tolerant input without an internal debouncer circuit. If the I ² C bus is disabled (ISEL = Low), then this pin selects the clock edge that will latch the data. How the EDGE setting works depends on whether dual or single edge latching is selected: <u>Dual Edge Mode (DSEL = High)</u> EDGE=Low: primary edge (first/even latch edge after DE is asserted) is the falling edge EDGE=High: primary edge (first/odd latch edge after DE is asserted) is the rising edge Note: In 24-bit single-clock dual-edge mode, EDGE is ignored. <u>Single Edge Mode (DSEL = Low)</u> EDGE=Low: the falling edge of the clock is used to latch data. EDGE=High: the rising edge of the clock is used to latch data.
DKEN	35	I	De-Skew Enable. <u>ISEL=High, DKEN=High</u> When the I ² C bus is enabled, this pin must be set High, DK[3:1] are ignored and the de-skewing increments are selected through the I ² C interface. <u>ISEL=Low, DKEN=High</u> When the I ² C bus is disabled, this pin enables the de-skewing increments to be read in through the DK[3:1] pins. <u>DKEN=Low, ISEL=Low</u> The default de-skew setting is used.

Input Voltage Reference Pin			
Signal Name	Pin #	Type	Description
VREF	3	AI	Input Reference Voltage. Selects the swing range of the digital parallel data inputs (D[23:0], DE, VSYNC, HSYNC, and IDCK). When VREF is HIGH, the digital parallel data inputs are normal high swing 3.3V inputs. When VREF is below 1.8V, the digital parallel data inputs are low swing inputs. In low swing mode, VREF must be set to ½ of V _{CCQ} .

Differential Data Out			
Signal Name	Pin #	Type	Description
TX0+	25	AO	Low Voltage Differential Signal Output Data Pair 0.
TX0-	24		
TX1+	28	AO	Low Voltage Differential Signal Output Data Pair 1.
TX1-	27		
TX2+	31	AO	Low Voltage Differential Signal Output Data Pair 2.
TX2-	30		
TXC+	22	AO	Low Voltage Differential Signal Output Clock Pair.
TXC-	21		
EXTSWING	19	AI	Voltage Swing Adjust. A resistor should be used to tie this pin to VCCA. The resistance determines the amplitude of the voltage swing. For remote display applications, 510Ω is recommended. For notebook computers, 680Ω is recommended.

Power Management			
Signal Name	Pin #	Type	Description
PD#	10	I	Power Down. If High, it indicates normal operation. If Low, it indicates power down mode. In power down mode, the digital core is powered down, but the digital input and output buffers and the I ² C interface are NOT disabled. Note that when ISEL = High, this pin should be tied Low to ensure the chip is powered off when Reset is asserted.

Reserved Pins			
Signal Name	Pin #	Type	Description
NC	34	-	Reserved. Must be tied low.

Power and Ground			
Signal Name	Pin #	Type	Description
VCC	1, 12, 33	P	Digital Power. 3.3V ±5%.
GND	16, 48, 64	P	Digital Ground. Connect to primary PCB ground plane.
VCCA	23, 29	P	Analog Power. 3.3V ±5%.
GND A	20, 26, 32	P	Analog Ground.
VCCPLL	18, 49	P	PLL Power. 3.3V ±5%.
GNDPLL	17	P	PLL Ground.

REGISTERS

Register Overview

The following table summarizes the I²C registers, documents the power-on default value (“Default”) and access type (“Acc”) for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), and “—” for "no access defined" (effectively RO) or for no power-up default value (read value undefined). Registers indicated as RW might have some read/only bits that always read back a fixed value (usually 0 if unimplemented / reserved).

Detailed register descriptions are provided on the following page of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Note 1: The only power-up defaults are the "Power Down" bit (Rx8[0]) and the "MSEN Source Select" bits (Rx9[6:4]). All other bits are undefined on power-up. All registers must be written at least once before normal operation can occur.

Note 2. Register RxC must be programmed to 89h for normal operation.

Table 3. I²C Register Summary

Offset	Register Name	Default	Acc
00	Vendor ID Low (VND_IDL)	06	RO
01	Vendor ID High (VND_IDH)	11	RO
02	Device ID Low (DEV_IDL)	92	RO
03	Device ID High (DEV_IDH)	31	RO
04	Device Revision (DEV_REV)	A0	RO
05	- reserved -	—	—
06	Low Frequency Limit (FRQ_LOW)	19	RO
07	High Frequency Limit (FRQ_HIGH)	64	RO
08	Miscellaneous Control 1	xxxxxxx0b	RW
09	Miscellaneous Control 2	x000xxxxb	RW
0A	Miscellaneous Control 3	—	RW
0B	Configuration Data (CFG)	D[23-16]	RO
0C	Must be set to 89h (VDJK)	—	RW
0D	Reserved (Do Not Program)	—	RW
0E	Reserved (Do Not Program)	—	RW
0F	Reserved (Do Not Program)	—	RW

I²C Register Descriptions

Offset 00 – Vendor ID Low (VND_IDL).....RO

7-0 Vendor ID [7:0].....always reads 06h

Offset 01 – Vendor ID High (VND_IDH)RO

7-0 Vendor ID [15:8].....always reads 11h

Offset 02 – Device ID Low (DEV_IDL).....RO

7-0 Device ID [7:0]always reads 92h

Offset 03 – Device ID High (DEV_IDH)RO

7-0 Device ID [15:8]always reads 31h

Offset 04 – Device Revision (DEV_REV).....RO

7-0 Device Revision [7:0]always reads A0h

Offset 06 – Low Frequency Limit (FRO_LOW).....RO

7-0 Low Frequency Limit [7:0]always reads 19h
1-pixel per clock mode (MHz)

Offset 07 – High Frequency Limit (FRQ_HIGH)RO

7-0 Low Frequency Limit [7:0]always reads 64h
1-pixel per clock mode (MHz) plus 65 MHz

Offset 08 – Miscellaneous Control 1.....RW

7-6 Reserved always reads 0

5 Vertical Sync Enable VEN

0 VSYNC is transmitted as fixed low

1 VSYNC input is transmitted as is

4 Horizontal Sync Enable..... HEN

0 HSYNC is transmitted as fixed low

1 HSYNC input is transmitted as is

3 Dual Edge Clock Select DSEL

Same function as DSEL input pin.

0 Single edge

1 Dual edge

2 Input Bus Width SelectBSEL

Same function as BSEL input pin.

0 Input data bus is 12 bits wide

1 Input data bus is 24 bits wide

1 Edge Select EDGE

Same function as EDGE input pin.

0 Input data is falling-edge-latched (falling edge latched first in dual-edge mode)

1 Input data is rising-edge-latched (rising edge latched first in dual-edge mode)

0 Power Down Mode.....PDB

Same function as the PD# input pin.

0 Power Downdefault

1 Normal operation

Offset 09 – Miscellaneous Control 2 RW

7 VLOW RO

This bit is a 0 if the VREF signal indicates low swing inputs.

6-4 MSEN Output Pin Source SelectMONSEL[2:0]

000 Force MSEN output high (disabled) default

001 Output the MDI bit (interrupt)

010 Output the RSEN bit (receiver detect)

011 Output the HTPLG bit (hot plug detect)

1xx -reserved-

3 Interrupt Generation Method.....MDISEL

0 Interrupt bit (MDI) is generated by monitoring MSEN

1 Interrupt bit (MDI) is generated by monitoring HTPLG

2 Receiver DetectRSEN

0 A powered-on receiver is not connected to the transmitter outputs

1 A powered-on receiver is connected to the transmitter outputs

This function is only available for use in DC-coupled systems.

1 Hot Plug Detect Input HTPLG

This bit reads the state of the HTPLG input pin.

0 Monitor Detect Interrupt MDI

0 Detection signal has changed logic level (write one to this bit to clear)

1 Detection signal has not changed state

Offset 0A – Miscellaneous Control 3 RW

7-5 De-Skew Setting (ignored if bit-4 = 0) DK[3:1]

000 1 step (minimum setup / maximum hold)

001 2 step

010 3 step

011 4 step

100 5 step recommended setting

101 6 step

110 7 step

111 8 step (maximum setup / minimum hold)

4 De-Skew Enable (through the DK inputs)DKEN

0 Disable

1 Enable

3-1 General Purpose Inputs..... CTL[3:1]

These bits read the state of the CTL[3:1] general-purpose input pins.

0 Reservedalways reads 0

Offset 0B – Configuration..... RO

7-0 Configuration [7:0] always reads the state of the D[23:16] inputs

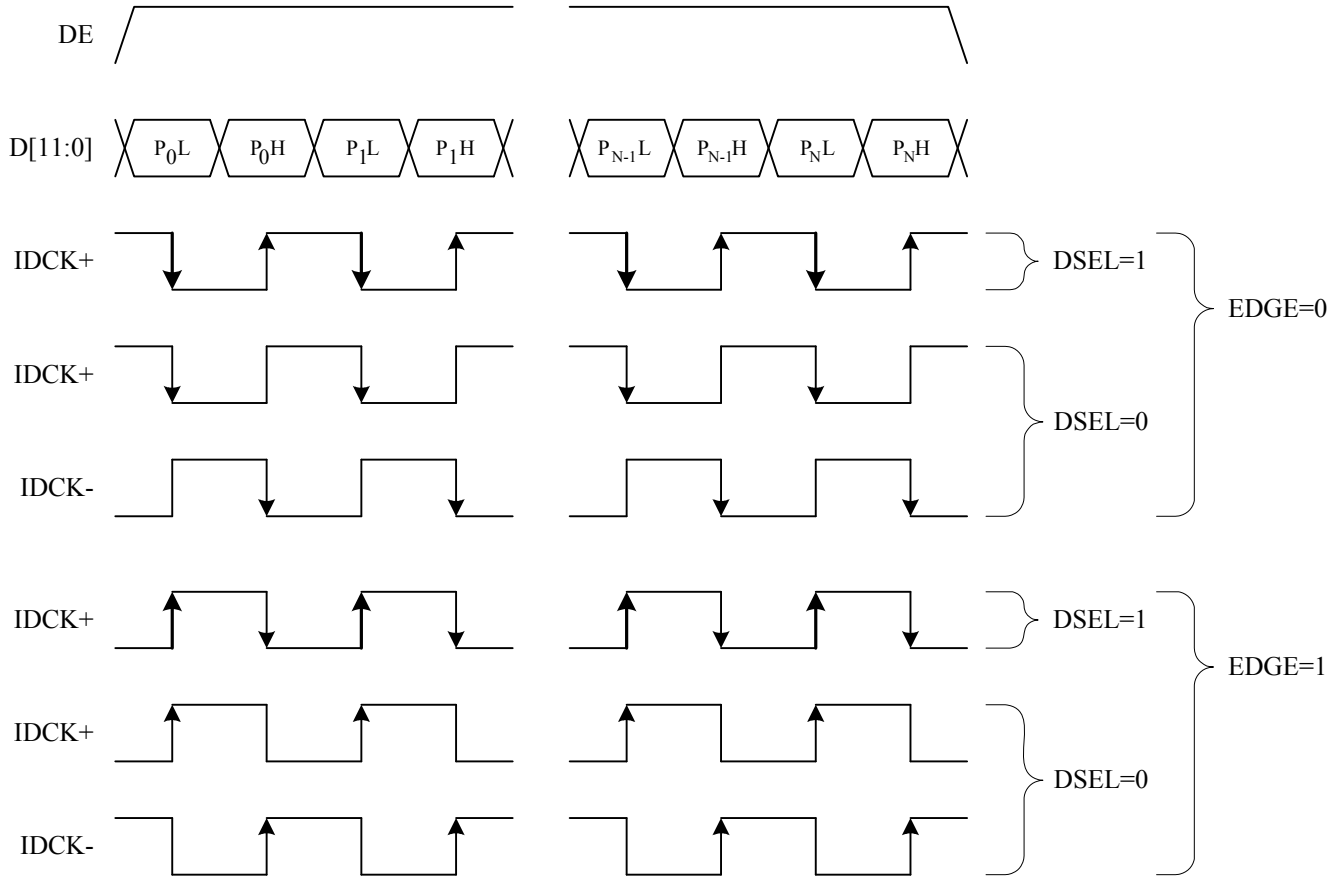


Figure 3. 12-bit Input Mode (BSEL=0)

Table 4. 12-bit Input Mode Data Mapping

Signal Name	P0		P1		P2	
	P0L	P0H	P1L	P1H	P2L	P2H
D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G2[3]	R2[7]
D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G2[2]	R2[6]
D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G2[1]	R2[5]
D[8]	G0[0]	R0[4]	G1[0]	R1[4]	G2[0]	R2[4]
D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B2[7]	R2[3]
D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B2[6]	R2[2]
D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B2[5]	R2[1]
D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B2[4]	R2[0]
D[3]	B0[3]	G0[7]	B1[3]	G1[7]	B2[3]	G2[7]
D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B2[2]	G2[6]
D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B2[1]	G2[5]
D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B2[0]	G2[4]

Note 1: Color Pixel Components: R=Red, G=Green, B=Blue

Note 2: Bit significance within a color: [7:0] = [msb:lsb]

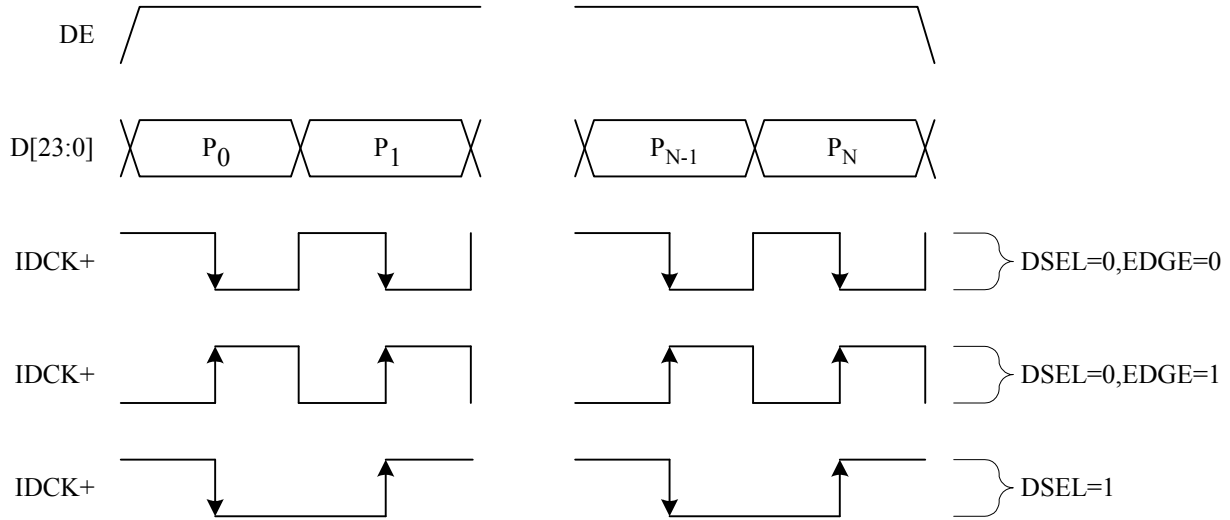


Figure 4. 24-bit Input Mode (BSEL=1)

Table 5. 24-bit Input Mode Data Mapping

Signal Name	P0	P1	P2
D[23]	R0[7]	R1[7]	R2[7]
D[22]	R0[6]	R1[6]	R2[6]
D[21]	R0[5]	R1[5]	R2[5]
D[20]	R0[4]	R1[4]	R2[4]
D[19]	R0[3]	R1[3]	R2[3]
D[18]	R0[2]	R1[2]	R2[2]
D[17]	R0[1]	R1[1]	R2[1]
D[16]	R0[0]	R1[0]	R2[0]
D[15]	G0[7]	G1[7]	G2[7]
D[14]	G0[6]	G1[6]	G2[6]
D[13]	G0[5]	G1[5]	G2[5]
D[12]	G0[4]	G1[4]	G2[4]
D[11]	G0[3]	G1[3]	G2[3]
D[10]	G0[2]	G1[2]	G2[2]
D[9]	G0[1]	G1[1]	G2[1]
D[8]	G0[0]	G1[0]	G2[0]
D[7]	B0[7]	B1[7]	B2[7]
D[6]	B0[6]	B1[6]	B2[6]
D[5]	B0[5]	B1[5]	B2[5]
D[4]	B0[4]	B1[4]	B2[4]
D[3]	B0[3]	B1[3]	B2[3]
D[2]	B0[2]	B1[2]	B2[2]
D[1]	B0[1]	B1[1]	B2[1]
D[0]	B0[0]	B1[0]	B2[0]

Note 1: Color Pixel Components: R=Red, G=Green, B=Blue

Note 2: Bit significance within a color: [7:0] = [msb:lsb]

Data De-Skew

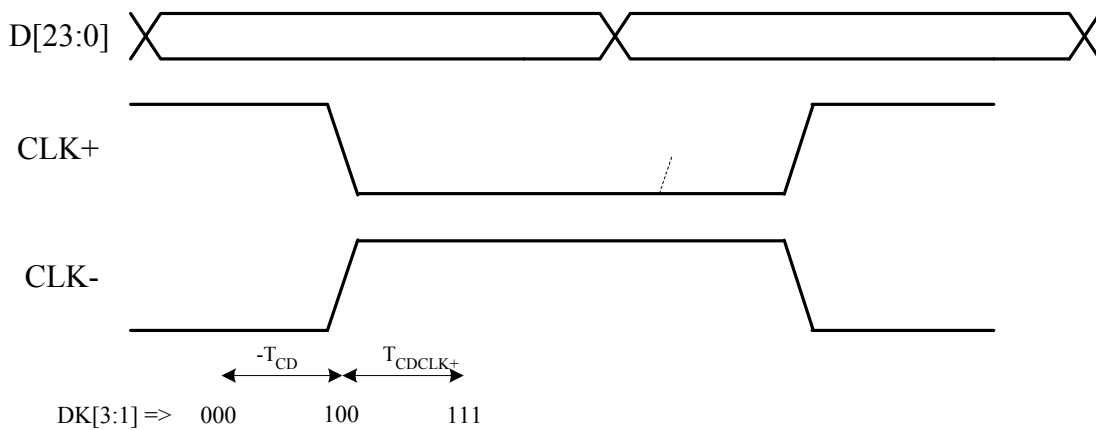
The de-skew feature can be used to adjust the input clock to data setup/hold time. Note that it is the clock that is being adjusted. Depending on whether DKEN is High or Low, it is possible to adjust the input setup/hold time using DK[3:1] or applicable I²C registers:

If DKEN is HIGH, DK[3:1] or specific I²C registers can be used to vary the input setup/hold time by an amount, T_{CD}, based on the following formula:

$$T_{CD} = (DK[3:1] - 4) \times T_{STEP} \text{ pSec}$$

Note: T_{CD} is the amount of setup/hold timing variation and DK[3:1] is the setting of the de-skew configuration signals or I²C registers. This feature is feasible for either 12-bit or 24-bit mode.

If DKEN is LOW and the VT1632A is not in I²C mode, the DK[3:1] inputs will be ignored, and then the default setting of T_{CD}=0 will be used.



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
T _{STG}	Storage Temperature	-40		125	°C
T _A	Ambient Operating Temperature	0		85	°C
V _{IN}	Input Voltage	-0.3		VCC+0.3	V
V _{OUT}	Output Voltage	-0.3		VCC+0.3	V
P _D	Package Power Dissipation			1	W
V _{ESD}	Electrostatic Discharge (Human Body)			2	kV
T _{VPS}	Vapor Phase Soldering (1 min.)			220	°C

Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC	Digital Supply Voltage	3	3.3	3.6	V
VCCA	Analog Supply Voltage	3	3.3	3.6	V
VCCPLL	PLL Supply Voltage	3	3.3	3.6	V
V _{CCN}	Supply Voltage Noise			100	mV _{P-P}
T _A	Ambient Operating Temperature	-10	25	70	°C

DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	High Swing High-level Input Voltage	2.0			V	$V_{REF} = V_{CCQ}$
V_{IL}	High Swing Low-level Input Voltage			0.8	V	$V_{REF} = V_{CCQ}$
V_{CCQ}	Low Swing Voltage	1		1.8	V	
V_{SH}	Low Swing High-level Input Voltage	$V_{CCQ}/2 + 0.3$			V	$V_{REF} = V_{CCQ}/2$
V_{SL}	Low Swing Low-level Input Voltage			$V_{CCQ}/2 - 0.1$	V	$V_{REF} = V_{CCQ}/2$
V_{CINH}	Input Clamp Voltage High			$VCC + 0.8$	V	$I_{CL} = +18mA$
V_{CINL}	Input Clamp Voltage Low			$GND - 0.8$	V	$I_{CL} = -18 mA$
I_{IL}	Input Leakage Current	-10		10	uA	
V_{OH}	Output High Voltage	$VCCA - 0.01$	$VCCA$	$VCCA + 0.01$	V	$R_{LOAD} = 50$
V_{OL}	Output Low Voltage	$VCCA - 0.60$		$VCCA - 0.40$	V	$R_{LOAD} = 50$
V_{REF}	Input Reference Voltage	0.5	$V_{CCQ}/2$	0.9	V	Low Swing
			V_{CCQ}			High Swing
V_{SWING}	Single Ended Output Peak-to-Peak Amplitude	510	550	590	mV	$R_{LOAD} = 50$ $R_{SWING} = 510$
I_{PD}	Power Down Current			0.1	mA	Inputs not toggling
I_{DOS}	Differential Output Short Circuit Current			0.5	uA	$V_{out} = 0$
I_{CCT}	Transmitter Supply Current		88		mA	IDCK = 165 MHz, Worst case pattern ¹ , 1 pixel per clock mode, $R_{LOAD} = 50$, $R_{SWING} =$ 510

Note 1: Black and white checkerboard pattern, each checker is one pixel wide

Note 2: VCCQ defines max voltage level of low sing input. It is not an actual input voltage.

Note 3: Assume all inputs to transmitter are not toggling.

AC Specifications

(Under normal operating conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Note
T _{CIP}	IDCK Period	6.06		40	ns	
F _{CIP}	IDCK Frequency	25		165	MHz	
T _{CIH}	IDCK High Time	2			ns	165 MHz
T _{CIL}	IDCK Low Time	2			ns	
T _{IIT}	IDCK Worst Case Clock Jitter			2	ns	
T _{SIDF}	Data, DE, V / H, CTL <u>Setup</u> Time to IDCK <u>Falling</u> Edge	1.0			ns	Single Edge
T _{HIDF}	Data, DE, V / H, CTL <u>Hold</u> Time to IDCK <u>Falling</u> Edge	0.9			ns	
T _{SIDR}	Data, DE, V / H, CTL <u>Setup</u> Time to IDCK <u>Rising</u> Edge	1.0			ns	
T _{HIDR}	Data, DE, V / H, CTL <u>Hold</u> Time to IDCK <u>Rising</u> Edge	0.9			ns	
T _{SID}	Data, DE, V / H, CTL <u>Setup</u> Time to IDCK <u>Falling / Rising</u> Edge	1.0			ns	Dual Edge
T _{HID}	Data, DE, V / H, CTL <u>Hold</u> Time to IDCK <u>Falling / Rising</u> Edge	0.9			ns	
T _{DDF}	HSYNC, VSYNC Delay From DE <u>Falling</u> Edge	1 T _{CIP}			ns	
T _{DDR}	HSYNC, VSYNC Delay From DE <u>Rising</u> Edge	1 T _{CIP}			ns	
T _{HDE}	DE High Time			819 T _{CIP}	ns	
T _{LDE}	DE Low Time	128 T _{CIP}			ns	
S _{LHT}	Small Swing Low-to-High Transition Time	170	200	230	ps	R _{LOAD} = 50 Ω , R _{SWING} = 510 Ω
S _{HLT}	Small Swing High-to-Low Transition Time	170	200	230	ps	



Figure 6. Input Data Transition Times

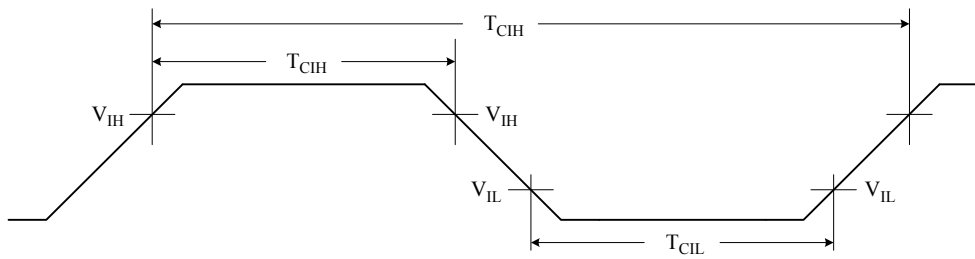


Figure 7. Input Clock Cycle / High / Low Times

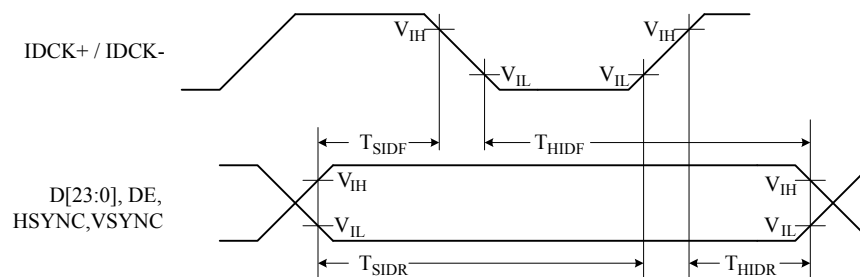


Figure 8. Control and Single-Ended Data Setup / Hold Times to IDCK+ / IDCK-

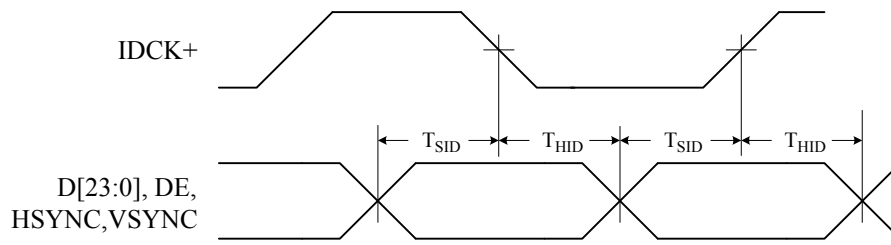


Figure 9. Dual-Edge Data Setup / Hold Times to IDCK+

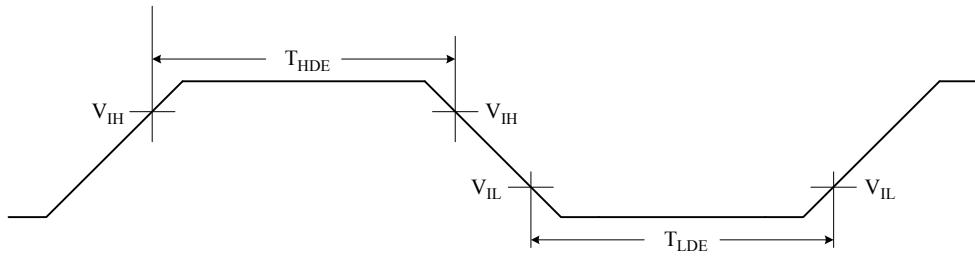


Figure 10. DE High / Low Times

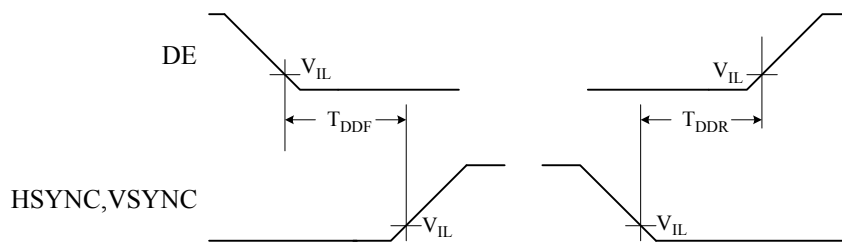
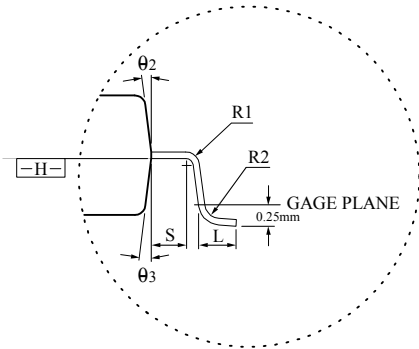
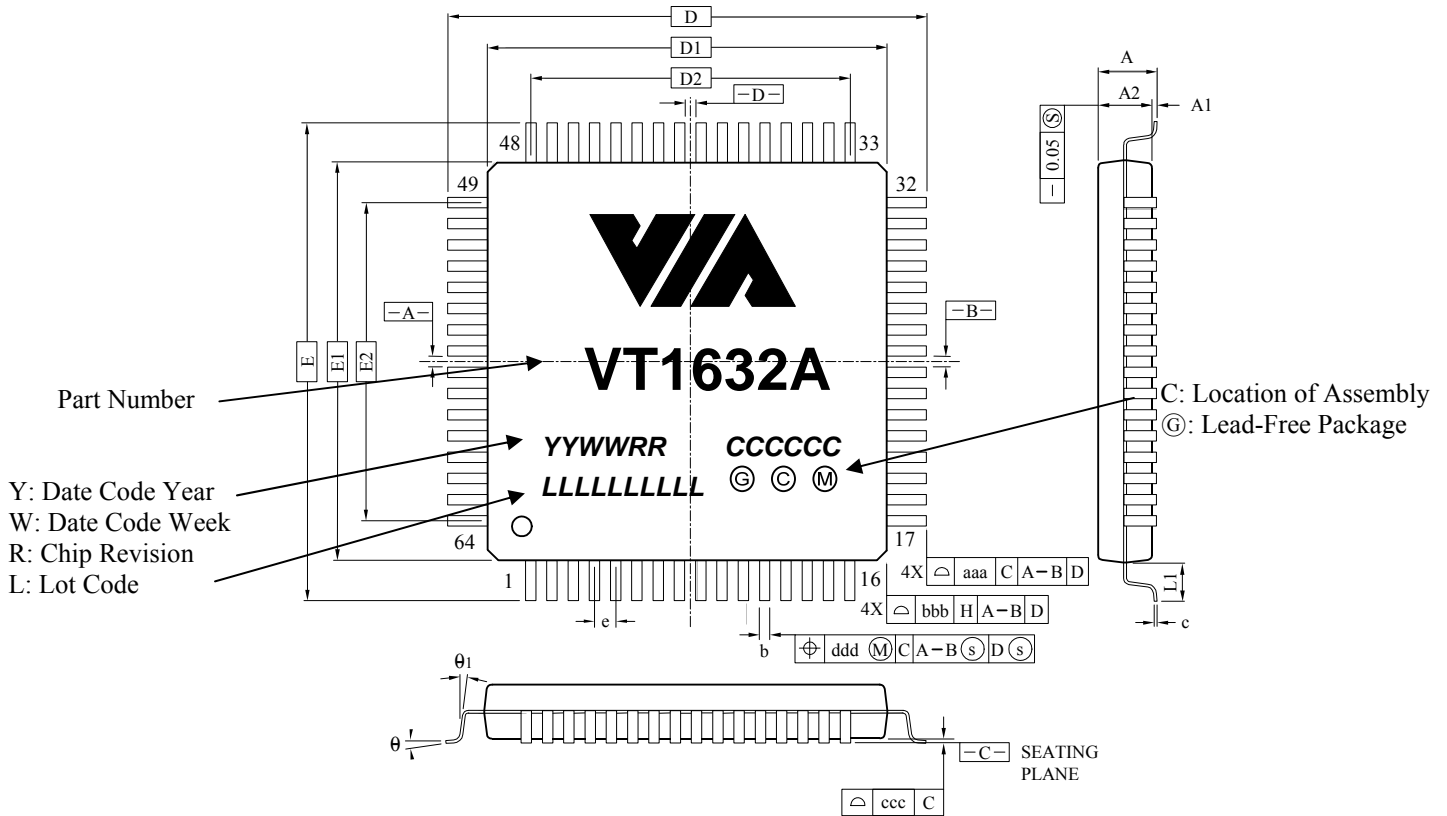


Figure 11. HSYNC / VSYNC Delay Times From / To DE





NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	12.00 BASIC			0.472 BASIC		
E	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.393 BASIC		
E1	10.00 BASIC			0.393 BASIC		
D2	7.50 BASIC			0.295 BASIC		
E2	7.50 BASIC			0.295 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ ₁	0	—	—	0	—	—
θ ₂	11	12	13	11	12	13
θ ₃	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 13. Lead-Free Mechanical Specification – 64-Pin TQFP Thin Quad Flat Pack

APPENDIX – REFERENCE DESIGN

Recommended routing guidelines are described in Appendix. Also, reference schematics for VT1632A DVI transmitter are attached (12-bit input mode with hardware strapping setting is used for P4M266; 24-bit input mode with I²C setting is used for CLE266).

PC Board Layout and Consideration

The VT1632A DVI transmitter supports the display from VGA to UXGA (1600 x 1200) resolutions with pixel clock supports 25 to 165MHz. It receives input data from graphic controller and then sends DVI link to LCD monitor. The connection is illustrated in Figure 14.

Figure 14. VT1632A Interconnection Diagram

Decoupling Capacitors

All high-speed active components should have capacitive decoupling on their supply lines, preferably very close to each power and ground pin. The optimum power supply decoupling is accomplished by placing a 0.1uF ceramic capacitor and a 10uF large storage capacitor to each of the power supply pins. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the VT1632A ground pins with ground pins of the decoupling capacitors then through a via to ground, as shown in Figure 15.

The ferrite bead is used to separate power planes (for noise or performance reasons). If one of the power planes generates a significant amount of noise, a ferrite and properly implemented decoupling capacitors can contain the noise within that local power plane and not allow it to propagate throughout the entire system’s power plane, or prevent outside noise from corrupting a sensitive power input. A ferrite bead is similar to an inductor in that it presents high impedance to high frequencies, but is different in that the impedance is mostly dissipative.

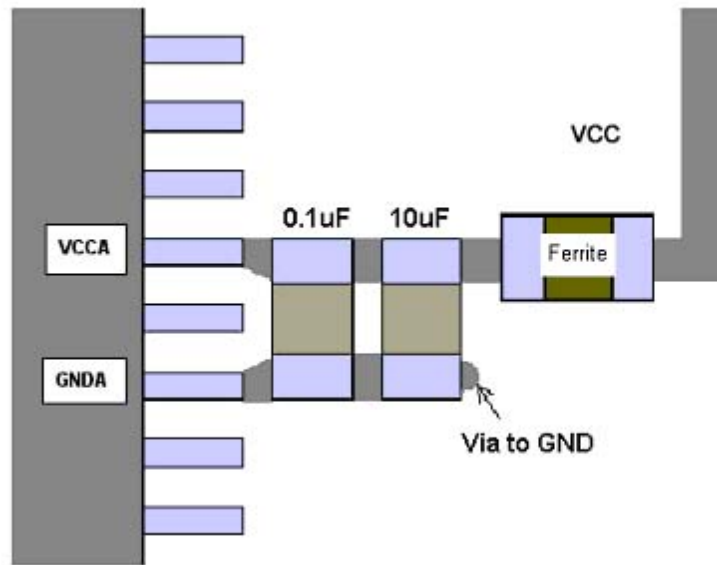


Figure 15. Decoupling Capacitors

Input Data

The IDCK+ and IDCK- are the critical paths that are capable of supporting up to 165MHz. This will reflect the quality of the display. The trace width should be between 6 and 15 mils. The routing should meet the 3-W rule (Width: Spacing=1:3) and refer to ground plane is strongly recommended.

DVI Link

The TX0+, TX0-, TX1+, TX1-, TX2+, TX2-, TXC+, TXC- are high frequency differential signals that need to be routed carefully. They must be routed in pairs: TX0+ and TX0-, TX1+ and TX1-, TX2+ and TX2-, TXC+ and TXC-.

- The length of the four pairs must be kept as close to the same as possible. The maximum length difference of them is recommended to be within 100 mils for any pair relative to each other.
- The number of bends should be kept to 4 or less and 45 degree is the maximum corner angle.
- Do not split the pairs and minimize the number of vias. Vias are very inductive and may cause phase delay problems.
- The recommended differential impedance for the transmission line is 100 ohm (50 ohm single-ended impedance).

The example of DVI link routing is shown in Figure 16.

The routing that is not recommended is shown in Figure 17. Note that:

- The routing of TX0 pair is not parallel.
- The TX1 pair is asymmetric via routing.
- The TXC pair is excessive via routing.
- The TX2 pair is separated and asymmetric via routing.

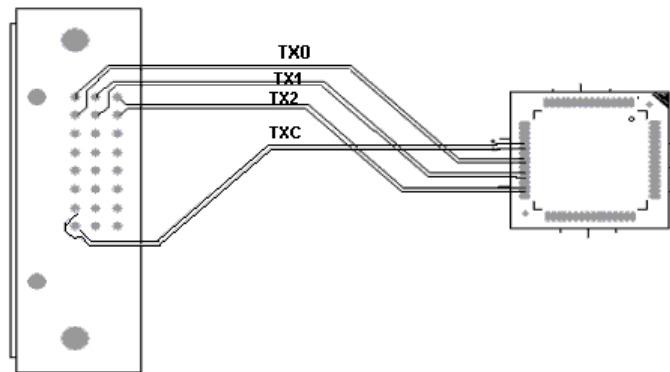


Figure 16. Routing of DVI Link

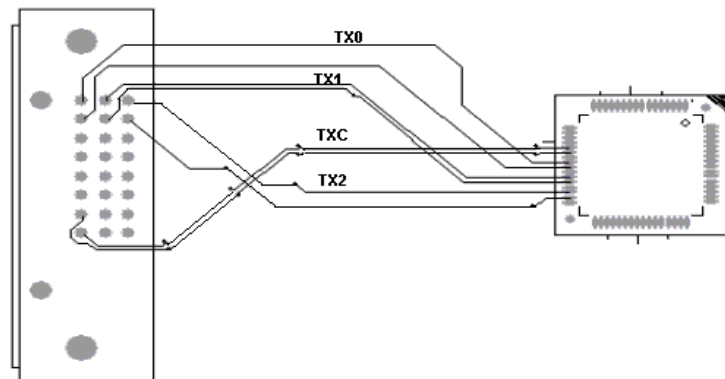


Figure 17. Not Recommended Routing